Board-level Functional Test Selection Based on Fault Tree Analysis

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***Abstract*—With the increasing complexity of the circuit board, the cost of the board-level functional test becomes dramatically high. Data-driven-based test selection methods have been widely studied for test-cost reduction. However, existing test selection methods tend to overfit due to overlooking the root causes of faulty boards. To address this issue, a test selection method based on fault tree analysis is proposed. A fault tree oriented to the board-level functional test is established for analyzing the reliability of the board and test items. The reliability analysis result is then utilized to design a test strategy. Three indices are introduced to evaluate the test efficiency and the test quality. Experimental results demonstrate the effectiveness of the proposed method.**

***Index Terms*—intelligent manufacturing, board-level functional test, test selection, fault tree analysis**

I. Introduction

With the rapid development of electronics and information technology, the electronic manufacturing industry has become increasingly important. Electronic devices have been playing an important role in both work and daily life. The quality of electronic devices is therefore essential and must be ensured before shipping. With the development of VLSI and semiconductor manufacturing technics, system on a chip is applied to various fields more and more widely. Therefore, the functions of electronic devices are mainly integrated into their boards [1], and quality testing of circuit boards is critical. The board-level functional test is the key procedure to ensure the board quality. With the increasing complexity of circuit boards, the cost of the board-level functional test becomes the main part of the test cost [2]. Therefore, designing an efficient strategy for the board-level functional test is essential.

Test ordering [3] [4] and test selection [5] [6] [7] are two major categories of methods for deriving test strategies. Test ordering is performed by testing items in a proper order, which can only reduce the test cost of faulty boards. Test selection means running chosen test items. The redundant tests are omitted to cut the test costs of faulty and fault-free boards. Since the board yield is relatively high in today's electronic industry [8], test selection is preferred over test ordering for designing board-level functional test strategies.

Existing test selection methods are based on data-driven modeling [8] [9] [10]. In practical scenarios, the performance of these methods depends on the quality of modeling data. As a result, the models tend to overfit, especially when evident process variations occur. The long-term accumulated rework data reflect the root causes of board faults. If the reliability of rework data is analyzed, the reliability of the board and test items can be derived. Based on the reliability analysis result, a robust test strategy that only the test item with low reliability can be designed to ensure the board quality with a relatively low time cost. Therefore, test selection methods based on reliability analysis are preferred for designing the test strategy.

Fault tree analysis (FTA) is a commonly used reliability analysis method [11]. Although there has been much effort on the board reliability by fault tree analysis, the board reliability has not been used for designing test selection methods. The related works on the board fault tree analysis can be classified

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into two categories. One mainly analyzes the faults caused by inappropriate settings during board fabrication processes [12] [13], while the other focuses on the faults of board modules [14]. However, neither of them analyzed the reliability of test items in the board-level functional test process. As test results are determined by the reliability of board components corresponding to the test items, fault tree analysis on the functional test process should be further studied.

In this paper, a board-level functional test selection method is proposed based on fault tree analysis. A laptop motherboard is taken as the object to illustrate the proposed method. The fault tree of the motherboard oriented to the board-level functional test is established by analyzing the root causes of the rework boards. The reliability analysis result is utilized for designing a test selection method to ensure the board quality with a relatively low test time cost. The test efficiency and test quality are evaluated by three indices, and the proposed method is validated by industrial data.

The rest of this article is organized as follows. In Section II, the FTA is introduced. In Section III, a fault tree of the laptop motherboard is established. In Section IV, a test selection method based on FTA is proposed and evaluation indices are introduced. In Section V, the effectiveness of the proposed method is demonstrated by a simulation experiment. This article is concluded in the last section.

II. A BRIEF INTRODUCTION TO FTA

As one of the widely used reliability analysis methods, FTA is often utilized to analyze the root causes of the undesired state of a system. In this article, FTA is performed to analyze the reliability of the circuit board and test items. The fault tree is established through a top-down approach, beginning with the identification of an undesired state, i.e. top event, followed by investigating the intermediate events and ending by analyzing the root causes, i.e. basic events. All kinds of events are linked by boolean logic symbols, such as the AND gate and OR gate.

If input events are all independent and are linked by the AND and OR gates, then the occurrence probability of the output event can be calculated as follows:

1) AND gate:

$$P_X = \bigcap_{i=1}^{n} P_{X_i} = \prod_{i=1}^{n} P_{X_i}, \tag{1}$$

where the output event X is linked with the input event X_i through an AND gate.

2) OR gate:

$$P_X = \bigcup_{i=1}^{n} P_{X_i} = 1 - \prod_{i=1}^{n} \left(1 - P_{X_i}\right), \tag{2}$$

where the output event X is linked with the input event X_i through an OR gate.

Suppose the system's undesired state is T, and basic events in the system are independent. If the basic event X_1 and the intermediate event M_1 occur at the same time will lead to the occurrence of T and the occurrence of the basic event X_2 or X_3 will lead to the occurrence of M_1. A fault tree can be established based on the suppositions above, as shown in Fig. 1.

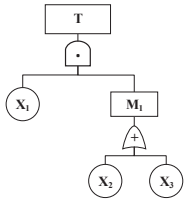

Fig. 1. Schematic example of a fault tree diagram

Each fault tree matches a particular Boolean expression. '$\cap$' in the Boolean expression means the relation of parallel (i.e. AND gate in the fault tree) and '$\cup$' means series (i.e. OR gate in the fault tree). Using the Boolean expression simplification formulas can simplify the Boolean expression of the fault tree in Fig. 1. The simplified Boolean expression is (3).

$$\begin{aligned} T &= X_1 \cap M_1 \\ &= X_1 \cap (X_2 \cup X_3) \end{aligned} \tag{3}$$

Let P_{X_i} denote the occurrence probability of the basic event X_i. The occurrence probability of the top event T can be expressed as P_T, which can be calculated with (1–2), as shown in (4).

$$P_T = P_{X_1}[1 - (1 - P_{X_2})(1 - P_{X_3})] \tag{4}$$

III. BOARD-LEVEL FUNCTIONAL TEST-ORIENTED FAULT TREE ANALYSIS

To address the issue of existing studies on board reliability analysis that overlook the direct cause of faulty boards and do not apply to test selection, this study establishes a fault tree tailored to the board-level functional test of a typical laptop motherboard. The root causes of defective tests are analyzed to create the fault tree. The circuit diagram of the laptop motherboard is presented in Fig. 2, and a brief overview of the fault tree's establishment for the laptop motherboard is provided.

During the board-level functional test procedure, a board is considered to be faulty if one or more test items fail. To calculate the reliability of the board and its test items, a fault tree is established, where the top event is the faulty board, and the intermediate events are the individual faulty test items. The top event is the union of intermediate events. The list of all board test items is presented in TABLE I.

To analyze the cause of the failing test items, the board is divided into four parts: Embedded Controller (EC) module, Central Processing Unit (CPU) module, Platform Controller Hub (PCH) module, and functional modules (e.g., Bluetooth module, FAN module, and Speaker module). The EC module contains an EC chip and EC BIOS, so the EC fault contains an EC chip fault and EC BIOS fault. The CPU module only

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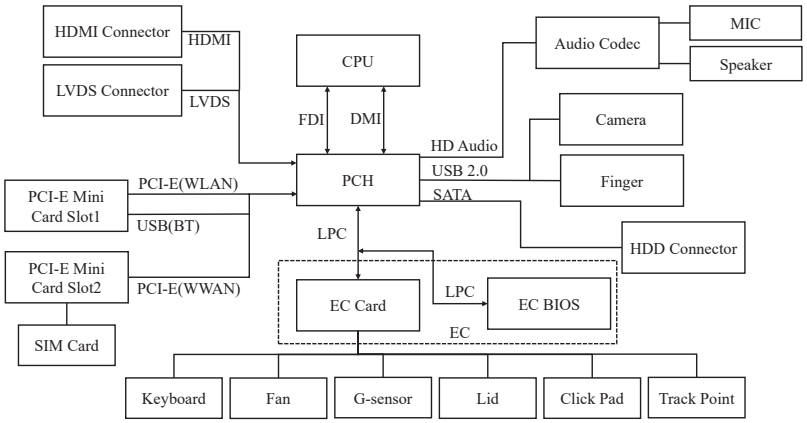

Fig. 2. The circuit diagram of a typical laptop motherboard.

TABLE I
THE TESTS OF A LAPTOP MOTHERBOARD

No.	Test item	No.	Test item
1	WWAN test	9	LVDS test
2	Keyboard test	10	Fingerprinter test
3	Fan test	11	Camera test
4	G-sensor test	12	Panel test
5	Lid test	13	Bluetooth test
6	Clickpad test	14	WLAN test
7	Trackpoint test	15	Speaker test
8	HDMI test	16	Microphone test

contains a chip, so the CPU fault means CPU chip fault. The board's functional modules can be categorized into two parts. The first is directly connected to the PCH module, while the second is connected via the EC module. Based on this categorization, two types of faults can occur in the PCH module. The first type, referred to as PCH module fault 1, is connected to two modules: one via the FDI and DMI buses to the CPU module, and the other via the LPC bus to the EC module. The second type, also known as PCH module fault 2, is connected directly to the CPU via the FDI and DMI buses.

Each functional test item in TABLE I matches a functional module of the board. Then the cause of the failed functional test item can be analyzed in two parts: the functional module fault and the fault of the module linked to the functional module.

The EC chip fault, CPU chip fault, and PCH chip fault mentioned above are all types of chip faults. During the board production process, components are typically soldered onto the printed circuit board, which can result in welding problems. Therefore, chip faults can include both chip damage and welding-related faults.

The causes of the failed functional test items are analyzed in the aforementioned procedure. The intermediate events in Fig. 2 are shown in TABLE II.

TABLE II
THE INTERMEDIATE EVENTS OF FTA

Symbol	Fault	Symbol	Fault
M_1	WWAN fault	M_{12}	Panel fault
M_2	Keyboard fault	M_{13}	Bluetooth fault
M_3	Fan fault	M_{14}	WLAN fault
M_4	G-sensor fault	M_{15}	Speaker fault
M_5	Lid fault	M_{16}	Microphone fault
M_6	Clickpad fault	M_{17}	PCH module fault 1
M_7	Trackpoint fault	M_{18}	PCH module fault 2
M_8	HDMI fault	M_{19}	PCH chip fault
M_9	LVDS fault	M_{20}	CPU fault
M_{10}	Fingerprinter fault	M_{21}	EC fault
M_{11}	Camera fault	M_{22}	EC chip fault

In TABLE II, the intermediate events M_1 to M_{16} denote the faults of functional test items. The intermediate events M_{17} to M_{22} denote the causes of the functional test fault, which need further analysis. Basic events, which are the root causes of the intermediate events M_{17} to M_{22}, are shown in TABLE III.

TABLE III
THE BASIC EVENTS OF FTA

Symbol	Fault	Symbol	Fault
X_1	Card reader fault	X_{13}	Bluetooth module fault
X_2	PCH pseudo soldering	X_{14}	Fan module fault
X_3	PCH chip damage	X_{15}	G-Sensor module fault
X_4	CPU pseudo soldering	X_{16}	Lid module fault
X_5	CPU chip damage	X_{17}	Clickpad module fault
X_6	EC BIOS fault	X_{18}	Trackpoint module fault
X_7	EC pseudo soldering	X_{19}	LVDS connector fault
X_8	EC chip fault	X_{20}	Camera module fault
X_9	Keyboard module fault	X_{21}	Speaker module fault
X_{10}	HDMI connecter fault	X_{22}	Microphone module fault
X_{11}	Finger Printer module fault	X_{23}	Audio Codec fault
X_{12}	HDD fault	X_{24}	WLAN module fault

The intermediate event of the keyboard fault is taken as an example to introduce the process of establishing the fault tree. The keyboard is connected to other components through the EC module, which is in turn connected to the PCH module

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through the LPC bus. As a result, the intermediate keyboard fault event is linked to the Keyboard module fault (i.e. basic event "X_9"), the EC fault (i.e. intermediate event "M_{21}"), and the PCH module fault 2 (i.e. intermediate event "M_{18}") through an OR gate. The PCH module is connected to the CPU module through the FDI and DMI buses. Therefore, the PCH module fault 2 is linked to both the CPU fault (i.e. intermediate event "M_{20}") and the PCH chip fault (i.e. intermediate event "M_{19}") through an OR gate. The EC fault is the union of the EC BIOS fault (i.e. basic event "X_6") and the EC chip fault (i.e. intermediate event "M_{22}"). Such fault tree branch aforementioned is shown in Fig. 3.

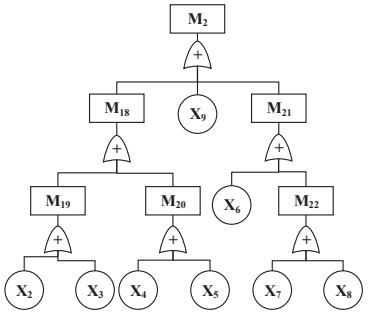

Fig. 3. Keyboard fault tree

Based on the analysis of the motherboard's circuit diagram, the fault tree of the typical laptop motherboard is established, as shown in Fig. 4.

In Fig. 4, T denotes the top event, the laptop motherboard fault. For simplicity, some fault tree branches of M_{17}, M_{18}, and M_{21} are omitted in Fig. 4.

Suppose the occurrence probability of the basic event X_i is P_{X_i}, then the Boolean expression of the fault test M_j in Fig. 4 and its occurrence probability is (5):

$$\begin{aligned} P_{M_j} &= P_{\bigcup_{X_i \in S_j} X_i} \\ &= 1 - \prod_{X_i \in S_j} (1 - P_{X_i}), \end{aligned} \tag{5}$$

where S_j is the set of all basic events of the corresponding intermediate event M_j. This set is shown in TABLE IV.

IV. Test Selection Method Based on Reliability Analysis

To implement the test selection method on the board-level functional test, we first need to determine the reliability of the board and each test item by utilizing the fault tree established in Section III. Once the reliability has been determined, we can set the threshold values for each test item to ensure the reliability of the board-level functional test. The defective rate is chosen as the primary reliability index to evaluate the quality of both the board and its test items. By comparing the actual defective rate of each test item during the production line testing to their respective threshold values, the decision to test or not can be made. This decision can be formulated as shown in (6):

TABLE IV
The Sets of Basic Events of Intermediate Events

Symbol	Intermediate event	Basic events
M_1	WWAN fault	$\{X_1, X_2, X_3, X_4, X_5, X_6, X_7, X_8\}$
M_2	Keyboard fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_9\}$
M_3	Fan fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{14}\}$
M_4	G-sensor fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{15}\}$
M_5	Lid fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{16}\}$
M_6	Clickpad fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{17}\}$
M_7	Trackpoint fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{18}\}$
M_8	HDMI fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{10}\}$
M_9	LVDS fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{19}\}$
M_{10}	Fingerprinter fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{11}\}$
M_{11}	Camera fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{20}\}$
M_{12}	Panel fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{12}\}$
M_{13}	Bluetooth fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{13}\}$
M_{14}	WLAN fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{24}\}$
M_{15}	Speaker fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{21}, X_{23}\}$
M_{16}	Microphone fault	$\{X_2, X_3, X_4, X_5, X_6, X_7, X_8, X_{22}, X_{23}\}$

$$s_i = \neg(\mu_i \leq \beta_i), \tag{6}$$

where $s_i \in \mathbb{Z}_2 = \{0, 1\}$ denotes the decision of test or not, 0 means not test, and 1 means test. μ_i denotes the index's actual value of the test item i counted on the production line, and β_i denotes the defective rate threshold of the test item i.

The test selection method based on the reliability analysis uses the fault tree of the board to obtain the range of the defective rate and then sets the corresponding threshold of the defective rate.

This article analyzes the reliable service data from board-level functional testing and calculates the occurrence frequency of basic events as probabilities, denoted by p_{X_i}. If the actual occurrence frequency of a basic event during the production line testing is less than p_{X_i}, the basic event is considered to be within the reliability range. Then, using (5) and the reliability range of the basic event, we can determine the reliability range of the test item j. The upper limit of this range is denoted by p_{M_j}:

$$\begin{aligned} P_{M_j} &= 1 - \prod_{i \in S_j} (1 - P_{X_i}) \\ &\leq 1 - \prod_{i \in S_j} (1 - p_{X_i}) \\ &\leq p_{M_j} \end{aligned} \tag{7}$$

p_{M_j} is taken as the defective rate threshold, that is, $\beta_i = p_{M_j}$ in (6).

At last, the test strategy, which means the decision of whether to test or not, can be made by comparing the actual value of the defective rate on the production line to the corresponding defective rate threshold by (6).

To assess the performance of the proposed method, three indices are utilized: average test time, defect level, and average test cost. The average test time refers to the time required to test a single board. The defect level indicates the proportion of defective boards that pass testing after using the test strategy.

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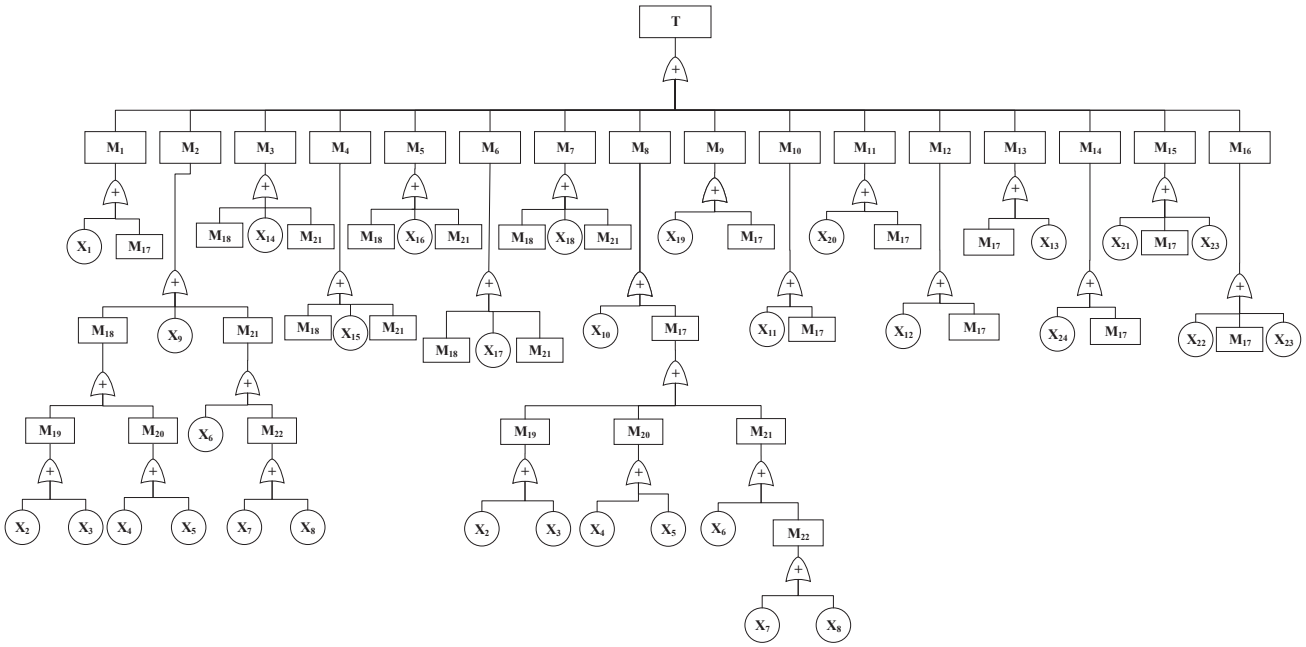

Fig. 4. The fault tree of the typical laptop motherboard

Both indices respectively gauge test efficiency and test quality. The test cost, on the other hand, measures the total test time and repair cost incurred by false positive boards. A false positive board is defined as a defective board that passes testing.

Suppose that there are n boards to be tested, and each containing m functional test items. The test results of each test item are recorded in a binary matrix $\boldsymbol{D} \in \mathbb{Z}_2^{n\times m}$, where 1 and 0 represent a passing or failing test, respectively. The average test time for each test item is stored in a vector $\boldsymbol{t} = [t_1, t_2, ..., t_m]^\mathsf{T}$, and a test strategy $\boldsymbol{s} = [s_1, s_2, ..., s_m]^\mathsf{T}$ is employed. The following indices can be calculated based on this information:

When the test strategy is determined, the test time of each board is the same, so f_1, the average test time of a single board, can be calculated as (8):

$$f_1 = \boldsymbol{t}^\mathsf{T}\boldsymbol{s} \tag{8}$$

The defect level denoted as f_2 is equal to the number of false positive boards divided by all boards that pass testing. Let w denote the average repair cost of each false positive board, then the average test cost denoted as f can be calculated as follows:

$$f = f_1 + wf_2 \tag{9}$$

V. Experiments

The real data are collected from a laptop manufacturing factory. To protect confidential information, the generated synthetic data are similar to the real test data. The synthetic data contains the test result of 16 test items of 1715 boards, the average test time of each test item, and the credible repair data.

The test result is stored in a matrix $\boldsymbol{D} \in \mathbb{Z}_2^{1715\times 16}$. The average test time of each test item is stored in a vector $\boldsymbol{t}$, whose length is 16. w in (9) can be set to 6 hours combined with the actual situation and expert experience.

Firstly, p_{X_i}, the occurrence probability of the basic event X_i, is calculated with the credible repair data. The occurrence probability of each basic event is shown in TABLE V.

TABLE V
THE PROBABILITIES OF BASIC EVENTS

Symbol	Probability(%)	Symbol	Probability(%)
X_1	0.0021	X_{13}	0.0021
X_2	0.0020	X_{14}	0.0022
X_3	0.0030	X_{15}	0.0019
X_4	0.0021	X_{16}	0.0019
X_5	0.0031	X_{17}	0.0019
X_6	0.0020	X_{18}	0.0022
X_7	0.0022	X_{19}	0.0022
X_8	0.0023	X_{20}	0.0022
X_9	0.0020	X_{21}	0.0023
X_{10}	0.0022	X_{22}	0.0022
X_{11}	0.0030	X_{23}	0.0021
X_{12}	0.0021	X_{24}	0.0022

Then, the probability's upper limit of the test item failing can be calculated with (7), TABLE IV, and TABLE V, which can be used as the defective rate threshold of each test item. The defective rate thresholds are shown in VI. The second

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column of this table shows the actual defective rate on the production line.

At last, the demonstration of the effectiveness of the test selection method based on reliability analysis is given in the following text.

The defective rate thresholds of the method proposed in this article are shown in TABLE VI. The current test selection method widely used in the industry is setting all defective rate thresholds to 500×10^{-6}. Comparing the defective rate threshold to the actual defective rate on the production line can obtain the test strategy shown in table VI. 1 and 0 in the test strategy represent testing or not respectively.

TABLE VI
THE TEST STRATEGIES OF THE PROPOSED METHOD AND THE CURRENT METHOD

Test item	DR[a](%)	Proposed method		Current method	
		DRT[b](%)	Test strategy	DRT[b](%)	Test strategy
WWAN test	0.0167	0.0184	0	0.0500	0
Keyboard test	0.0200	0.0183	1	0.0500	0
Fan test	0.0333	0.0185	1	0.0500	0
G-sensor test	0.0233	0.0182	1	0.0500	0
Lid test	0.0200	0.0182	1	0.0500	0
Clickpad test	0.0233	0.0182	1	0.0500	0
Trackpoint test	0.0067	0.0185	0	0.0500	0
HDMI test	0.0000	0.0185	0	0.0500	0
LVDS test	0.0200	0.0185	1	0.0500	0
Fingerprinter test	0.0200	0.0193	1	0.0500	0
Camera test	0.0200	0.0185	1	0.0500	0
Panel test	0.0200	0.0184	1	0.0500	0
Bluetooth test	0.0033	0.0184	0	0.0500	0
WLAN test	0.0600	0.0185	1	0.0500	1
Speaker test	0.0467	0.0206	1	0.0500	0
Microphone test	0.0500	0.0205	1	0.0500	0

[a]Abbreviations of defective rate.
[b]Abbreviations of defective rate threshold.

The corresponding indices the average test cost, the average test time, and the defect level are calculated with (8–9), as shown in TABLE VII.

TABLE VII
THE THREE INDICES OF THE PROPOSED METHOD AND THE CURRENT METHOD

Index	Current method	Proposed method
Average test cost (s/board)	74.049	51.824
Average test time (s/board)	4.929	46.064
Defect level (%)	0.3202	0.0268

According to the experiments, the FTA-based test selection method detects more faulty boards, thereby reducing the defect level and significantly lowering repair costs. The proposed method reduces the test cost by 30.01% compared to the current test selection method widely used in the industry. Moreover, the proposed method sets an effective test strategy for test items through reliability analysis rather than based on the expert experience.

VI. CONCLUSION

A board-level functional test selection method based on fault tree analysis is proposed in this article. A board-level functional test-oriented fault tree is developed to analyze the reliability of the boards and test items based on the root causes of defective boards. An effective testing strategy is then derived to improve the test performance. Three indices are introduced to evaluate the effectiveness of the proposed method. Experimental results show that the proposed method is capable of ensuring the board reliability at a low test cost compared to an industrial selection method. The proposed method provides an effective solution for efficient and reliable board-level functional test-cost reduction.

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